BM-STP4953

Dual P Channel Enhancement Mode MOSFET

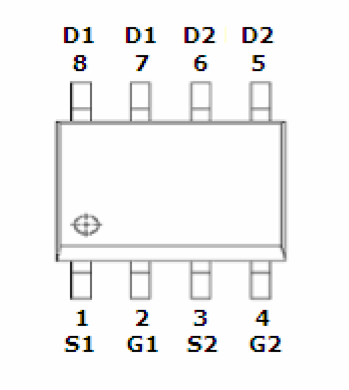
-5.0A

DESCRIPTION

BM-STP4953 is the dual P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD backlight, notebook computer power management, LCD-TV , LCD- Monitor and other battery powered circuits.

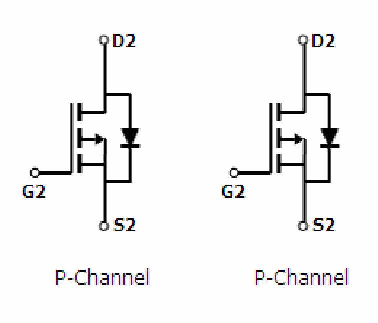
PIN CONFIGURATION

SOP-8



FEATURE

- -30V/-5.0A, $R_{DS(ON)}$ = 65mΩ @V_{GS} =-10V
- -30V/-4.4A, $R_{DS(ON)}$ = 85mΩ @V_{GS} = -6.0V
- -30V/-3.8A, $R_{DS(ON)}$ = 95mΩ @V_{GS} = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design



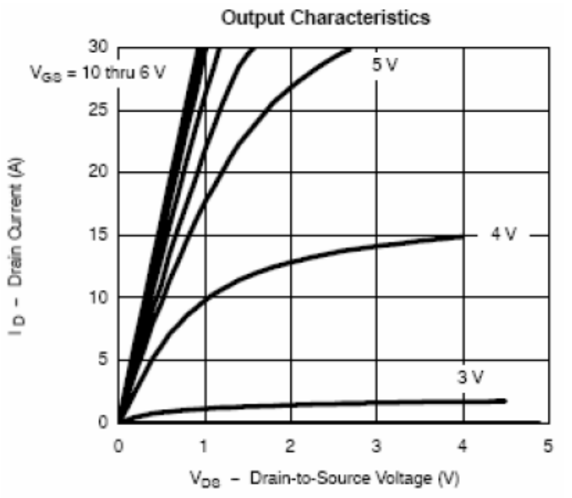
ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		**Symbol**	Typical	**Unit**
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (TJ=150℃)	T_A=25℃ T_A=70℃	I_D	-5.0 -4.0	A
Pulsed Drain Current		I_{DM}	-30	A
Continuous Source Current (Diode Conduction)		I_S	-2.3	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	2.7 1.8	W
Operation Junction Temperature		T_J	-55/150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	70	℃/W

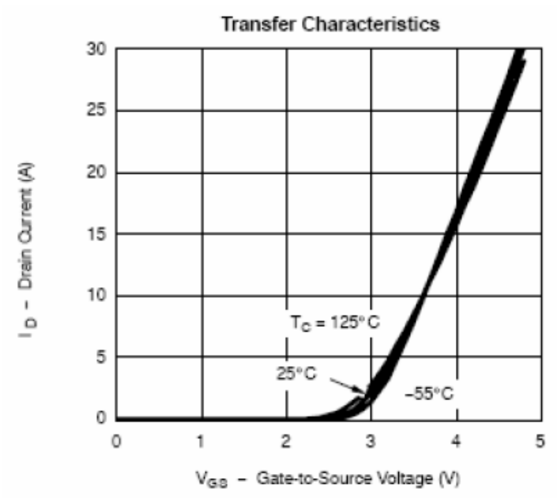
ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250 uA	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS} T_J=55℃	V_{DS}=-30V,V_{GS}=0V			-1	uA
		V_{DS}=-30V,V_{GS}=0V			-5	
On-State Drain Current	$I_{D(on)}$	V_{DS}=-5V,V_{GS}=10V	-25			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-5.0A V_{GS}=-6.0V, I_D=-4.4A V_{GS}=-4.5V,I_D=-4.0A		0.55 0.65 0.85	0.65 0.85 0.95	Ω
Forward Tran Conductance	gfs	V_{DS}=-10V,I_D=-5.0A		9.0		S
Diode Forward Voltage	V_{SD}	I_S=-2.0A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V,V_{GS}=-10V I_D≡-5.0A		15	10	nC
Gate-Source Charge	Q_{gs}			4.0		
Gate-Drain Charge	Q_{gd}			2.0		
Input Capacitance	Ciss	V_{DS} =-15V,VGS=0V f=1MHz		680		pF
Output Capacitance	Coss			120		
Reverse TransferCapacitance	Crss			75		
Turn-On Time	$t_{d(on)}$	V_{DD}=15V,R_L=15Ω I_D=-1.0A,V_{GEN}=-10V R_G=6Ω		7.0	15	nS
	t_r			10	20	
Turn-Off Time	$t_{d(off)}$			40	80	
	t_f			20	40	

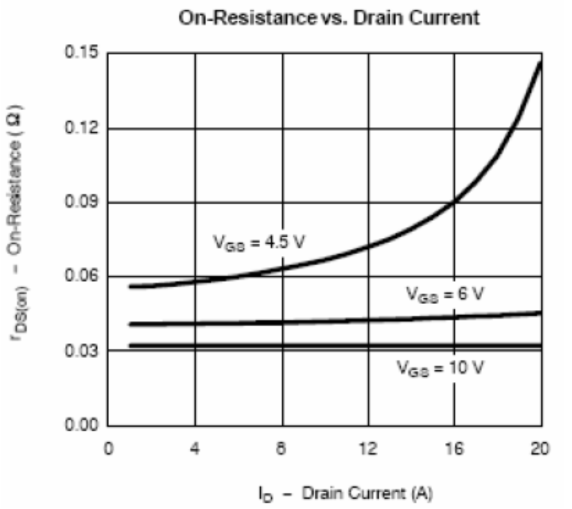
TYPICAL CHARACTERICTICS (25℃ Unless Note)



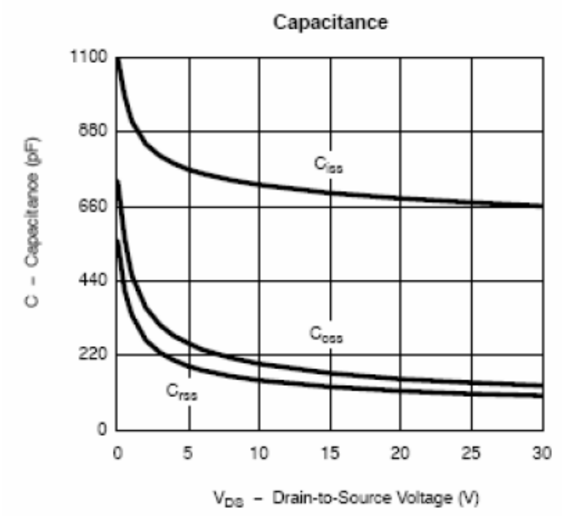
Output Characteristics



Transfer Characteristics

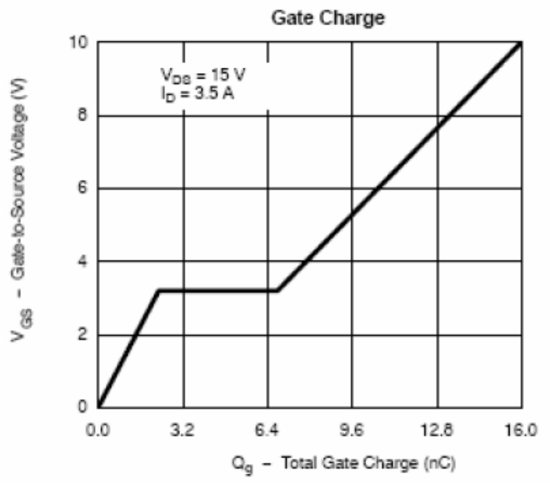


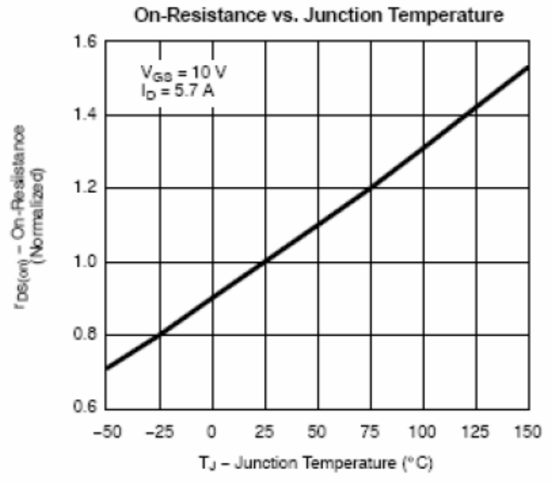
On-Resistance vs. Drain Current

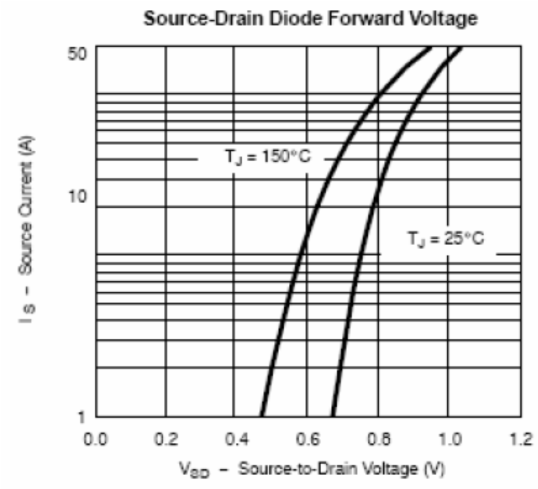


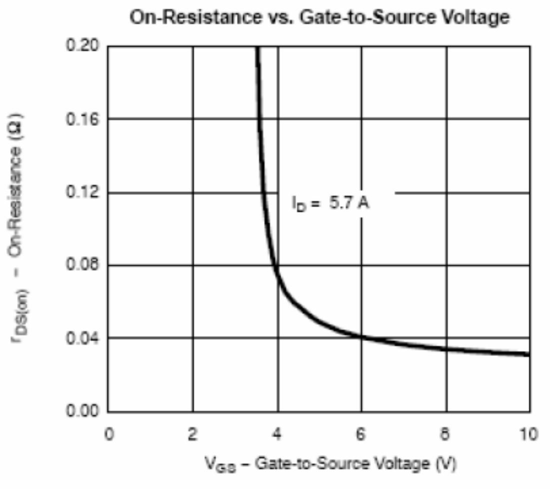
Capacitance

TYPICAL CHARACTERICTICS (25℃ Unless Note)

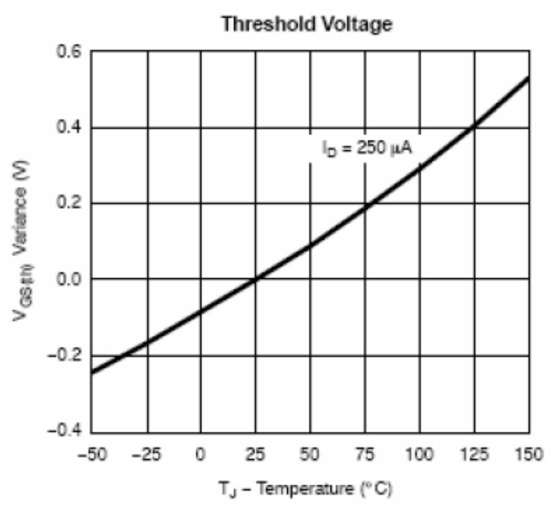

Gate Charge

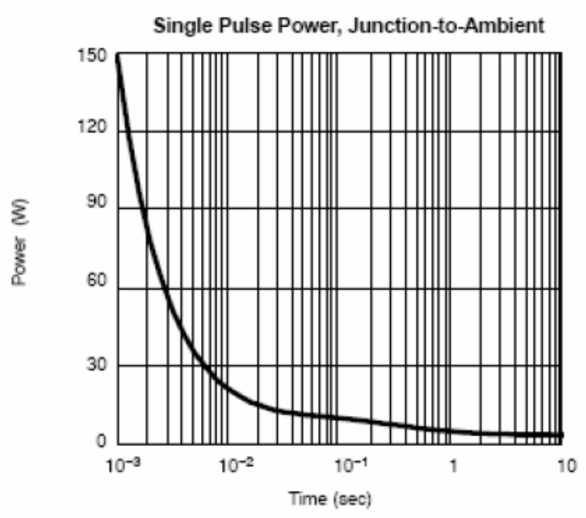

On-Resistance vs. Junction Temperature

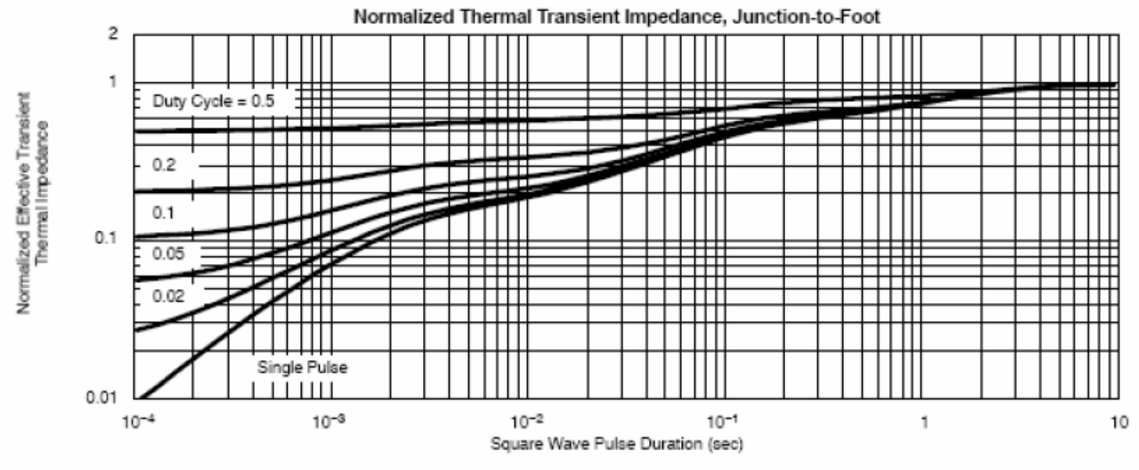

Source-Drain Diode Forward Voltage


On-Resistance vs. Gate-to-Source Voltage

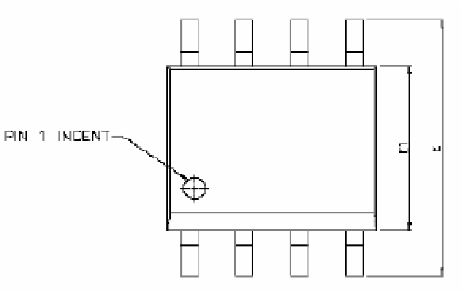
TYPICAL CHARACTERICTICS (25℃ Unless Note)

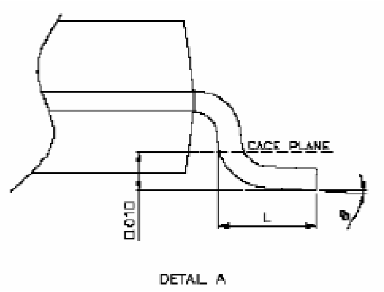


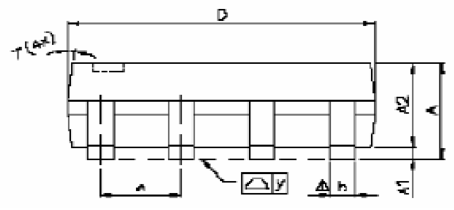


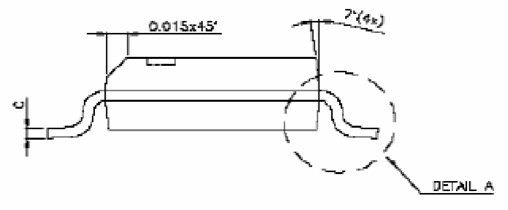


SOP-8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
△2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°